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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,753	11/16/2001	Heeloo Chung	3981-26	3370

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,753	CHUNG ET AL.	
	Examiner	Art Unit	
	Derrick W. Ferris	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-38 and 40-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-38 and 40-44* is/are rejected.

7)☒ Claim(s) *10 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/2/2006 has been entered.

Response to Arguments

2. This Office action is in response to applicant's paper filed 8/2/2006. **Claims 1-44** as originally filed are still pending.

3. Examiner does not **withdraw** the current anticipated and obviousness rejections to *Wynee*. In particular, applicant's affidavit is insufficient for the following reasons provided below. Since applicant paid for a continued examination, the current Office action is made non-final. In addition, in order to expedite the prosecution of the case, the examiner has provided a new rejection(s) shown below with respect to the broadly claimed subject matter.

Affidavit

4. The declaration under 37 C.F.R. 1.131 filed on 1/23/2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the *Wynee et al.* and *Tran* references.

5. The evidence submitted is insufficient to establish applicant's alleged actual reduction to practice of the invention in this country or a NAFTA or WTO member country after the effective date of the *Wynee et al* reference.

With respect to items 6 and 7 of applicant's declaration and Exhibit A, it is unclear where the claimed subject matter is supported in the Exhibits. In particular, the examiner found no evidence that Exhibit A teaches at least an input for receiving packets of data, *each packet associated with an output queue* or equivalent. Specifically, the above issue is where the factual evidence is found *in Appendix A* to support the claim recitation above. With respect to applicant's remarks, applicant makes reference to the above statement in the second declaration at paragraphs 6-10 on page 2. Specifically, applicant references pages 16-17 of Exhibit A with respect to the source header information for the Cougar ASIC. As such, page 16 of the exhibit shows the source of the packet header as the Cheetah. However, no factual evidence was provided in the appendix to further support applicant's comments about the Cheetah interface at paragraph 6 of the second declaration as to how it relates to the invention. Thus it is unclear from the factual evidence provided that the Cheetah is "an input for receiving packets, each packet associated with an output queue" (or equivalent) as recited in the claims. Instead, applicant appears to only make an assertion of the above statement in the last sentence of paragraph 7 but does not provided any further factual evidence in the appendix. In addition, the information provided on pages 16-17 of Exhibit A show packet header information for a Cougar interface but makes no reference that the packet header format is an "F10 header" as taught by the rest of the Exhibit.

In addition, the examiner found no evidence that Exhibit A teaches at least an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility *to output queues, and store one or more packets associated with output queues into blocks assigned to those output queues* or equivalent for the same reason as mentioned

above. In particular, there is no further description with respect to the figure shown on page 12 of the exhibit. Thus it is unclear that "p1a" is a part "a" of a "packet 1" as argued by applicant. Again, the examiner found no factual evidence supported in the appendix.

In conclusion, the rejections are maintained since not enough factual evidence was provided in the declaration.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-4, 6, 7, 11, 15-17, 19, 22-27, 29, 32-38, 41, and 42** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application 2003/0016686 A1 to *Wynee et al.* ("*Wynee*").

As to **claim 1**, see e.g., figure 2b where the input for receiving packets of data, each packet associated with an output queue is taught e.g., as the protocol processor 20. Specifically, the protocol processor 20 segments the received packet(s) on bus 12a into cells and then stores the sequence of cells in internal memory using traffic manager 22. The packet is associated with an output queue based on the flow ID of the packet which reflects the VOQ of the packet. An intermediate storage facility having a plurality of blocks is taught as cell memory 32, see e.g., figure 32. An intermediate storage facility

manager is taught e.g., as traffic manager 22 or as data path controller 30 and queuing system 36. As such, traffic manager 22 or data path controller 30 and queuing system 36 are configured to assign particular blocks of the intermediate storage facility to output queues, and store one or more packets associated with output queues into the blocks assigned to those output queues. In particular, cells are stored in blocks and given a BLOCK_ID.

As to **claim 2**, the pointer repository is taught as the queue used to store the BLOCK_IDs (i.e., pointers). A trunk manager is taught e.g., as also data path controller 30 and queuing system 36 where the trunk is the packet flow.

As to **claim 3**, packets are broken down into one or more cells, these cells are stored in blocks in cell memory 32 and then outputted to a common output port corresponding to a VOQ.

As to **claim 4**, the cells are stored prior to entering the traffic manager 22, see e.g., paragraphs 0036-0038 on page 3.

As to **claim 6**, see e.g., paragraph 0037 on page 3.

As to **claim 7**, the second storage facility is the traffic manager for the output port, see e.g., figure 2b with respect to figure 3. The intermediate storage manager is traffic manager 26 or data path controller 30 and queuing system 36. A command is the LOAD command as taught by the reference.

As to **claim 11**, the output queue manager is the traffic manager 26 or data path controller 30 and queuing system 36

As to **claim 15**, see similar rejection to claim 1. In particular, since the traffic manager 22 or data path controller 30 and queuing system 36 are configured to assign particular blocks, they are configured to sort the data packets into groups, see e.g., paragraph 0042 on page 4.

As to **claim 16**, see similar rejection to claim 3.

As to **claim 17**, the block storage memory is cell memory 32 and the block storage memory manager coupled to the buffer memory manager is data path controller 30.

As to **claim 19**, the second block storage memory is output queues 37 shown e.g., in figure 3 which is coupled to the data path controller (i.e., buffer memory manager).

As to **claim 22**, each cell is stored in internal memory, see e.g., paragraph 0035 before being sent to the traffic manager.

As to **claim 23**, see e.g., figures 2a and 2b where the protocol processors 20 and 28 are the packet processors coupled to one or more of the input ports and output ports.

As to **claim 24**, see similar rejection to claim 1. In addition, note that the switch fabric is cross-point switch 16 shown e.g., in figure 1. Also note that the routing controller 18 is responsible for a scheduler configured to direct the packet buffer memory to output the groups through the switch fabric, see e.g., paragraph 0035 on page 3.

As to **claim 25**, see similar rejection to claim 16.

As to **claim 26**, see similar rejection to claim 17.

As to **claim 27**, see e.g., see e.g., figure 3 where the command is the read/write command.

As to **claim 29**, see similar rejection to claim 19.

As to **claim 32**, see similar rejection to claim 24.

As to **claim 33**, see similar rejection to claim 3.

As to **claim 34**, see similar rejection to claim 17.

As to **claim 35**, see similar rejection to claim 1.

As to **claim 36**, the list of blocks are stored by the queuing system 36, see e.g., figure 4.

As to **claim 37**, the predetermined group is based on the flow ID (i.e., FIN). As such, the data path controller 30 also reads from the memory device or cell memory 32.

As to **claim 38**, see similar rejection to claim 7.

As to **claim 41**, each flow is related by a block ID.

As to **claim 42**, the added pointers are the block ID values, see e.g., paragraph 0044 on page 4.

8. **Claims 1-9, 11-38, and 40-44** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,687,247 B1 to *Wilford et al.* ("*Wilford*").

As to **claim 1**, the buffer manager is taught as control element 130, see e.g., figure 2. An input for receiving packets of data, each packet associated with an output queue is taught as packets entering the inbound receiver 220. An intermediate storage facility having a plurality of blocks is taught as inbound packet buffer 245 and output packet buffer 280. In particular, once packets are sent to an inbound receiver they are further stored in inbound packet buffer 245 and output packet buffer 280 where the packet has a modified header. In addition, see e.g., virtual output queuing with respect to the Memory

Controller (MCC) ASIC at e.g., column 25, lines 37-50. With respect to a plurality of blocks, see e.g., figures 16a and 16b with respect to the structure of the memory and in particular note the "chunks" shown in figure 16b. As such, with respect to an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility to output queues, and store one or more packets associated with the output queues into blocks assigned to those output queues, see e.g., figure 16b. In particular, each queue is assigned 16 KB blocks, see e.g., bottom of column 28 and top of column 29. As such, packet data is stored in 64 byte cells. Each cell is stored as a burst of 4 to a single memory bank in one memory module. Consecutive cells in a packet/TX queue are stored in memory banks interleaved across two memory modules. Eight cells across all banks equals one 512 byte chunk. Consecutive chunks equals one block. TX output queues are made of link lists of 16 KB blocks. See e.g., column 31, lines 45-60.

As to **claim 2**, see e.g., column 9, lines 4-15.

As to **claim 3**, see e.g., column 31, lines 45-60 with respect to the queue structure.

As to **claim 4,** see e.g., FIFO buffer at e.g., top of column 7.

As to **claim 5**, see e.g., top of column 29.

As to **claim 6**, see e.g., column 28, lines 37-51.

As to **claims 7-8**, see e.g., figure 16b.

As to **claim 9**, see e.g., CAR which uses tokens.

As to **claim 11**, see e.g., figure 16b.

As to **claim 12**, see e.g., top of column 29.

As to **claim 13**, see e.g., figure 16b.

As to **claim 14**, see e.g., top of column 29.

As to **claim 15**, see similar rejection to claim 1. As to sorting the packets, see e.g., storing the information in the various memory banks.

As to **claim 16**, the functionality within the inbound receiver.

As to **claim 17**, see e.g., figures 16a and b and column 31, lines 45-61.

As to **claims 18-19**, see similar rejection to claim 8.

As to **claim 20**, see similar rejection to claim 14.

As to **claim 21**, network 1 is the Internet.

As to **claim 22**, see similar rejection to claim 4.

As to **claim 23**, for the packet processor, see e.g., the control element 130.

As to **claim 24**, see similar rejection to claim 1. In addition, see e.g., the switch fabric 120 shown e.g., in figure 2.

As to **claim 25**, see similar rejection to claim 16.

As to **claim 26**, see similar rejection to claim 17.

As to **claim 27**, the command is the information sent to the MMC.

As to **claim 28**, see similar rejection to claim 18.

As to **claim 29**, see similar rejection to claim 19.

As to **claim 30**, see similar rejection to claim 14.

As to **claim 31**, see similar rejection to claim 21.

As to **claim 32**, see similar rejection to claim 24.

As to **claim 33**, see similar rejection to claim 16.

As to **claim 34**, see similar rejection to claim 17.

As to **claim 35**, see similar rejection to claim 1.

As to **claim 36**, blocks of information are connected in link-lists by pointers, see e.g., top of column 9.

As to **claim 37**, see e.g., column 29, lines 35-45.

As to **claim 38**, see similar rejection to claim 19.

As to **claim 40**, see e.g., top of column 9.

As to **claims 41-42**, see e.g., column 29, lines 35-44.

As to **claim 43**, see similar rejection to claim 20.

As to **claim 44**, see e.g., top of column 44.

9. **Claims 1, 15, 24, 32, and 35** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,757,795 B2 to *Barri et al.* ("*Barri*").

As to **claim 1**, the buffer manager is shown e.g., in figure 1a. An input for receiving packets of data, each packet associated with an output queue is taught as packets/frames entering the flexbus4. An intermediate storage facility having a plurality of blocks is taught as the memory in the dataflow chip 14 and specifically the memory system 21 shown in figure 1b. Also see e.g., column 3, lines 44-48 with respect to queuing a data frame. In particular, with respect to a plurality of blocks, see the structure of the memory shown in figure 3. As such, with respect to an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility to output queues, and store one or more packets associated with the output queues into

blocks assigned to those output queues, the structure of the memory shown e.g., in figure 3. The intermediate storage facility manager is taught e.g., as memory arbiter 24.

As to **claim 15**, see similar rejection to claim 1. Output ports are taught as the sending the information out of the flexbus 4'. Data is further sorted into groups based on the slices as shown e.g., in figures 3 and 4.

As to **claim 24**, see similar rejection to claim 15. With respect to the switch fabric, see e.g., column 3, lines 55-59. The scheduler is further part of the receiver controller 22 and the transmitter controller 36.

As to **claim 32**, see similar rejection to claim 24.

As to **claim 35**, see similar rejection to claim 1.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 5, 12, 14, 20, 30, 43 and 44** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application 2003/0016686 A1 to *Wynee et al.* ("*Wynee*") in view of U.S. Patent Application No. 2003/0084246 A1 to *Tran et al.* ("*Tran*").

As such to **claim 5**, *Wynee* discloses limitations in the base claim.

Wynee is silent or deficient to the further limitation us using a SRAM circuit.

Tran teaches the further recited limitation above at e.g., figure 3 with respect to buffer memory 31.

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Wynee* by clarifying that the cell memory 32 is the a SRAM circuit.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation for modifying the reference or to combine the reference teachings would be because SRAM circuits are inexpensive. In particular, *Tran* cures the above-cited deficiency by providing a motivation found at e.g., paragraph 0006 on page 1. Second, there would be a reasonable expectation of success since both references teach storing cells (see e.g., paragraph 0028 on page 2 of *Tran*. Thus the references either in singular or in combination teach the above claim limitation(s).

As to **claims 12**, see similar rejection to claim 5.

As to **claims 14**, see similar rejection to claim 5. In addition see e.g., figure 3 of *Tran* with respect to output SDRAM controller e.g., as state machine 40.

As to **claims 20**, see similar rejection to claim 5.

As to **claim 30**, see similar rejection to claim 5.

As to **claim 43**, see similar rejection to claim 5.

As to **claim 44**, the limitation is met since when the cell is ready to be sent it is stored in cell memory such that the amount of data stored in the blocks of the memory device is equal to a threshold.

12. **Claims 21 and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application 2003/0016686 A1 to *Wynee et al.* ("*Wynee*") in view of "Data and Computer Communications" to *William Stallings* ("*Stallings*").

As such to **claim 21**, *Wynee* discloses limitations in the base claim.

Wynee is silent or deficient to the further limitation of the Internet. In particular, *Wynee* teaches the transmission of packets.

Stallings teaches the further recited limitation above at page pages 28-29 since packets are known to traverse the Internet.

The proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Wynee* by clarifying that packets are transmitted over a network where the network is the Internet.

As such, examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the above limitation. In particular, the motivation for modifying the reference or to combine the reference teachings would be to allow different parties to communicate with one another over a known network such as the Internet. In particular, *Tran* cures the above-cited deficiency by providing a motivation found at e.g., page 28 since a known set of networks is the Internet.

As to **claim 31**, see similar rejection to claim 21.

Allowable Subject Matter

13. **Claims 10, and 39** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (571) 272-3123. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571)272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Derrick W. Ferris
Examiner
Art Unit 2616

DWF

9/24/04

DERRICK W. FERRIS
PRIMARY PATENT EXAMINER